Analysis of High-Speed GaAs Source-Coupled FET Logic Circuits

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Abstract—**A source-coupled FET logic (SCFL) circuit is proposed for gigabit rate digital signal processing. FET threshold voltage tolerance in the SCFL circuit and the SCFL circuit performance are presented. The speed of the SCFL gate depends on the operating region of the FET. For high-speed operation, FET's drain-to-source voltage higher than a pinchoff voltage has to be supplied. The SCFL gate, which is composed of 1.5-μm gate-length FET's, shows that the minimum propagation time is predicted to be 25 ps/gate. Minimum rise time and fall time are expected to be 54 ps and 51 ps, respectively. Maximum *RZ* data rate is expected to be 5.6 Gb/s. The SCFL circuit is applicable for high-speed digital signal processing.**

I. Introduction

DIGITAL GaAs IC'S are expected to enable gigabit rate signal processing. These GaAs IC's are composed of normally on and/or normally off MESFET's. Typical normally on MESFET IC's are buffered FET logic (BFL) [1] and Schottky diode FET logic (SDFL) [2]. One of the well-known normally off MESFET IC's is direct-coupled FET logic (DCFL) [3]. To improve a weak point in DCFL, low pinchoff voltage FET logic (LPFL) is proposed [4]. Up to the present, DCFL has shown the highest speed, 29 ps/gate at room temperature [5]. To realize higher speed GaAs IC's with these conventional circuit configurations, the MESFET gate length must be reduced to sub-micron dimensions. However, a fabrication process for GaAs IC's composed of submicrometer gate MESFET's is not complete. In addition to gate length, one of the factors which has effects on both propagation time and transition time is gate-to-drain capacitance C_{gd}. This capacitance reduces with an increase in drain-to-source voltage V_{ds} [6]. In conventional circuits (BFL, SDFL, and DCFL), it is difficult to reduce C_{gd} sufficiently. The reason is that V_{ds} for driver FET only sets logic-swing voltage and must be lower than the pinchoff voltage when an FET is switched on. On the other hand, these bias points are adjustable in current mode logic (CML) circuits [7]. CML [8], which consists of bipolar transistors, resistors, and level shift diodes, is well known. The present CML circuit consists of GaAs MESFET's, resistors, and level shift diodes. This GaAs MESFET CML is called a source-coupled FET logic (SCFL). This paper describes high-speed SCFL circuit analysis.

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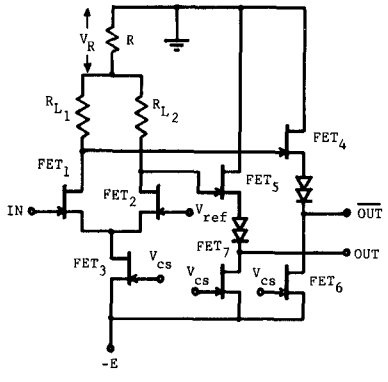

Fig. 1. GaAs MESFET CML gate configuration.

II. Source-Coupled FET Logic Configurations

An actual SCFL configuration is shown in Fig. 1. The input terminal is FET_1, gate and output terminals are drains of FET_6 and FET_7. A reference voltage V_{ref} is applied to the FET_2 gate. When the FET_1 gate voltage is equal to V_{ref}, the same magnitude of the current flows through FET_1 and FET_2 to ground. At an input voltage higher than V_{ref}, the current mostly flows through FET_1. At an input voltage lower than V_{ref}, the current mostly flows through FET_2. The reference voltage sets the logic threshold level. The state of the SCFL can be detected from the resultant voltage drop across R_{L_1} or R_{L_2}. The net voltage swing is determined by the value of the resistors and the magnitude of the current. Further, these two values are chosen to accomplish charging and discharging of all the parasitic capacitances at the desired switching rate. Consequently, at the drain of FET_1, an output that is the complement of its input is obtained. At the drain of FET_2, the same sign output as input is obtained.

The features of the SCFL circuit are as follows. First, if FET's threshold voltage from wafer to wafer is scattered, operating point and output voltage swing can be optimized by controlling V_{ref} and V_{cs}. Second, for many fan-outs, an SCFL circuit is capable of driving the following gate because of source–follower buffers. Third, a fan-in increase reduces a transition region in transfer characteristic and brings an increase in transfer gain. Output voltage swing and output voltage level are unaffected, due to the use of a constant current source.

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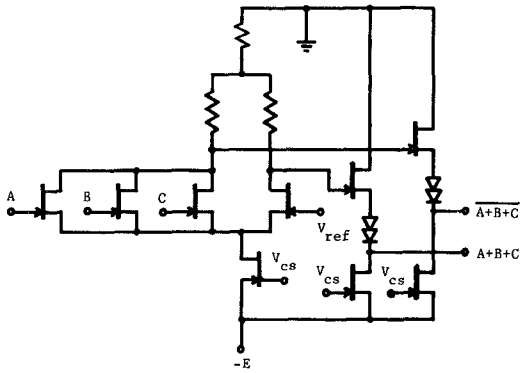
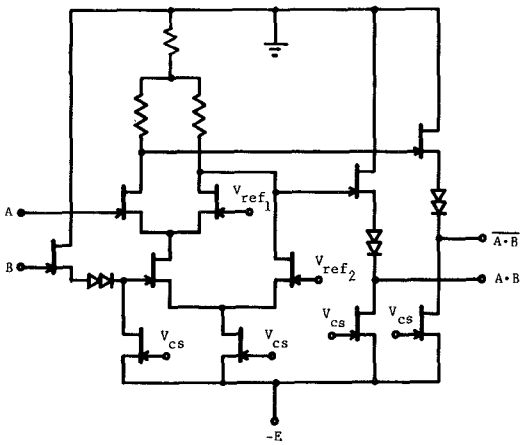
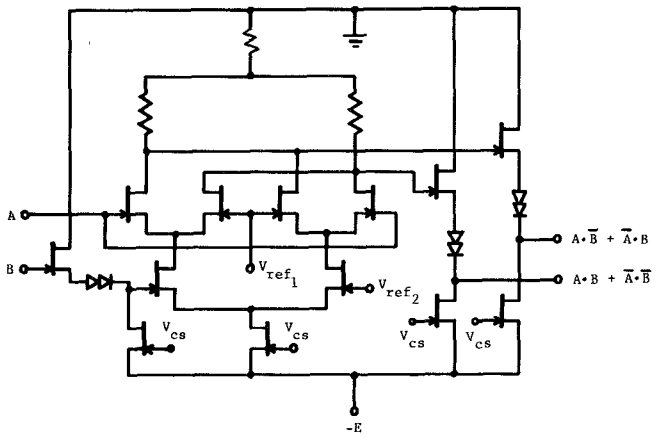


Fig. 2. Three-input OR/NOR SCFL gate.



(a)



(b)

Fig. 3. Series gate circuits. (a) AND/NAND SCFL gate. (b) Exclusive OR/NOR SCFL gate.

To compose an OR/NOR gate from this configuration, another FET is added in parallel to FET_1, as shown in Fig. 2. An AND/NAND gate and an Exclusive-OR/NOR gate, which are similar series-gate configurations to bipolar CML circuits, are shown in Fig. 3(a) and (b), respectively. In these actual configurations, it is necessary to set V_{ref_1}, V_{ref_2}, V_{cs}, and $-E$. A network which generates these bias voltages has to be included in GaAs IC chips for general purposes.

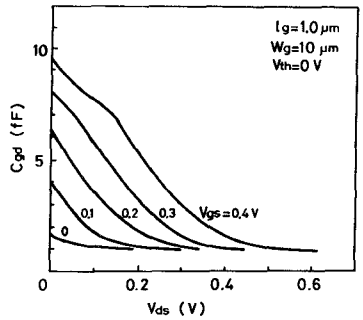


Fig. 4. Drain-to-source bias dependence of drain-to-gate capacitance for various gate-to-source voltage.

III. Operating Points and Threshold Voltage for High-Speed Operation

For high-speed operation, one of the most important FET parameters is a transition frequency f_T. An FET with high f_T can quickly steer the current in SCFL circuits. Therefore, f_T of FET has to take the large value. An f_T is given by the following equation. The detailed calculation process is shown in Appendix I

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})}. \tag{1}$$

The various quantities used in this equation are defined as follows:

g_m transconductance;
C_{gs} gate-to-source capacitance, which depends on gate-to-source bias voltage;
C_{gd} gate-to-drain capacitance, which depends on gate-to-drain bias voltage.

In order to increase f_T, C_{gs} and C_{gd} have to decrease. C_{gs} takes the minimum value at the gate-to-source voltage lower than V_{th}, and C_{gd} takes the minimum value when V_{ds} is higher than the pinchoff voltage, according to works by Shur [9], Curtice [10], or our results of two-dimensional device simulation in Fig. 4. For high-speed operation, the FET's operating region has to be contained within the V_{ds} range higher than the pinchoff voltage. By appropriately setting reference voltage V_{ref}, which can adequately control the logic threshold level, the FET's operating region can be optimized. In Fig. 1, threshold voltage V_{th} for FET_1 and FET_2 has to satisfy the following condition derived from Appendix II:

$$V_{th} \geq 1.5V_{sw} + V_{ref} + V_R \tag{2}$$

where V_{sw} is a voltage swing at the drains of FET_1 and FET_2, V_{ref} is a reference voltage, and V_R is a voltage drop across resistor R.

Threshold voltage V_{th} for FET_4 and FET_5 is given as follows:

$$V_{th} \geq -V_R. \tag{3}$$

FET_3, FET_6, and FET_7, which act as current sources, have to be biased by V_{ds} larger than the pinchoff voltage. From Appendix II, threshold voltages of FET_3, FET_6, and FET_7

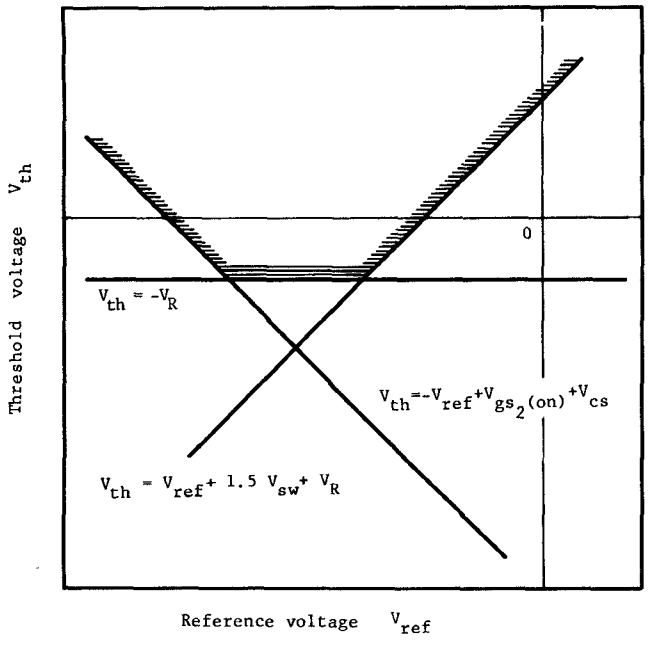


Fig. 5. Contours of threshold voltage for high-speed operation.

are given as follows. When each V_{th} has the same value

$$V_{th} \geq V_{cs} - V_{ref} + V_{gs_2(on)} \tag{4}$$

where $V_{gs_2(on)}$ is the FET_2 gate-to-source voltage when input level is low.

On the other hand, the transfer gain has to be larger than unity. Inverter gain is given as the average between common mode gain and differential mode gain [11]. Inverter gain is approximately shown as $g_m R_{L_1}/2$. From that condition, the following relation is given:

$$g_m R_{L_1}/2 > 1. \tag{5}$$

From (2), (3), and (4), relations between V_{th} and V_{ref} are as shown in Fig. 5. The SCFL operating bias region for high-speed logic is indicated by the hatched lines. Minimum V_{th} exists in Fig. 5. This minimum value is equal to $-V_R$. The type of FET, enhancement, and/or depletion is not a serious problem.

For example, when an SCFL circuit consists of FET's, which give $I-V$ characteristics in Fig. 6, calculated transfer characteristics with ASTAP [12] are shown in Fig. 7. Individual parameters are given in Table I.

The dynamic performance of this SCFL chain (four stages) is also calculated with ASTAP. In this simulation, the present FET model is composed of a dc model, which is represented by the current source, capacitance model, and Schottky gate diode model [13]. Using this FET model, close agreement between the observed and calculated delay of an inverter chain was obtained. The FET model is shown in Fig. 8. Propagation delay time per gate t_{pd} is obtained by a half of the total time across a chain of two gates in four-stages SCFL. Rise time t_r and fall time t_f are estimated by third-stage output waveform. The reason is that single-stage performance is dependent upon input

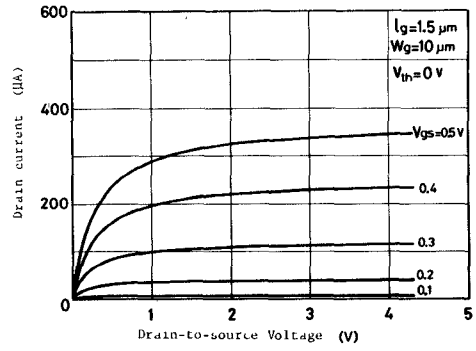


Fig. 6. FET $I-V$ characteristics for SCFL circuits simulation. Horizontal: 1 V/div. Vertical: 100 μA/div. Step: 0.1 V. Dimensions: gate length = 1.5 μm, gate width = 10 μm, drain-to-source spacing = 6 μm. Electrical parameter: Threshold voltage = 0 V.

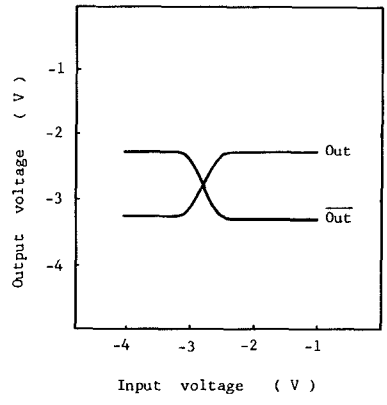


Fig. 7. Calculated transfer characteristics for an SCFL.

TABLE I
PARAMETERS IN AN SCFL CIRCUIT

FET Number	Gate Width	3	1.5×150 μm²
1	10 μm	4	do.
2	do.	Diode Parameters	
3	do.	Ideality factor n = 1.18	
4	22	Saturation current $J_0 = 7.78\times10^{-8}$ A/cm²	
5	do.		
6	10	Barrier height ϕ = 0.77 eV	
7	do.	Series resistance R = 80 Ω	
		Resistor	Magnitude
Diode Number	Area	R	3.0 KΩ
1	1.5×150 μm²	R_{L1}	4.5
2	do.	R_{L2}	do.

pulse waveform in simulation. Reference voltage dependence of t_{pd}, t_r, and t_f is shown in Fig. 9. If minimum t_{pd} is 25 ps/gate, then t_r and t_f are 54 ps and 51 ps, respectively. Values of t_{pd}, t_r, and t_f are not sensitive to a reference

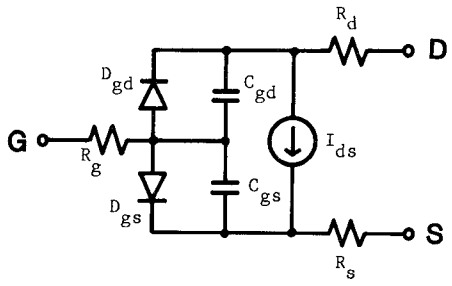


Fig. 8. MESFET model for digital circuit analysis.

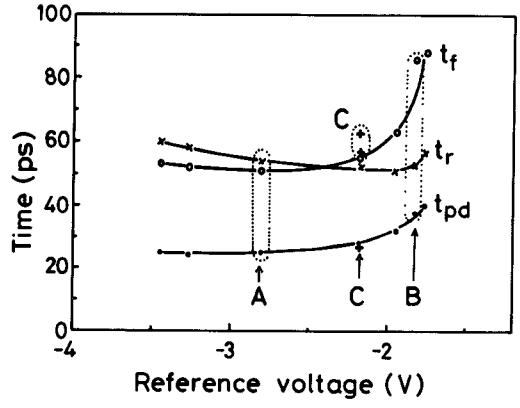


Fig. 9. Reference voltage dependence for delay t_{pd}, rise time t_r, and fall time t_f. Bias conditions of A, B, and C correspond to waveforms A, B, and C in Fig. 10, respectively.

voltage increase. This result indicates a wide tolerance for the reference voltage.

Output waveforms under the various operating conditions are shown in Fig. 10. Output waveform A is obtained under optimum operating conditions. Typical electrical parameters are: $V_{\text{ref}} = -2.81$ V, $V_{sw} = 1.0$ V, $V_R = 0.6$ V, $V_{cs} = -5.2$ V, and $V_{gs_2(\text{on})} = 0.4$ V. These parameters satisfy (2), (3), and (4). t_{pd}, t_r, and t_f are 25 ps/gate, 54 ps, and 51 ps, respectively. Waveform B is given under optimum conditions, except for the reference voltage, which is -1.83 V. The other parameters are: $V_{sw} = 1.0$ V, $V_R = 0.6$ V, $V_{cs} = -5.2$ V, $V_{gs_2(\text{on})} = 0.4$ V. These parameters satisfy (3). t_{pd}, t_r, and t_f are 38 ps/gate, 53 ps, and 86 ps, respectively. Waveform C is obtained under optimum conditions, except for the source–follower FET operating region. Resistor R in Fig. 1 falls to zero. V_{ref} and V_{sw} are -2.18 V and 1.0 V, respectively. V_{cs} and $V_{gs_2(\text{on})}$ are -5.2 V and 0.4 V, respectively. These parameters satisfy (2) and (4). t_{pd}, t_r, and t_f are 27 ps/gate, 63 ps, and 57 ps, respectively. Waveform A shows the shortest transition times and the shortest propagation time. The undershoot of waveform B is due to leakage of a high-frequency component of the input signal through gate-to-drain capacitance. The leakage depends on the gate-to-drain capacitance increase. A slight increase in propagation time and transition time in waveform C is due to an input capacitance increase in source–follower FET. The input capacitance increase is mainly derived from a gate-to-drain capacitance increase in the source-follower FET. When two types of single-current pulse sequence,

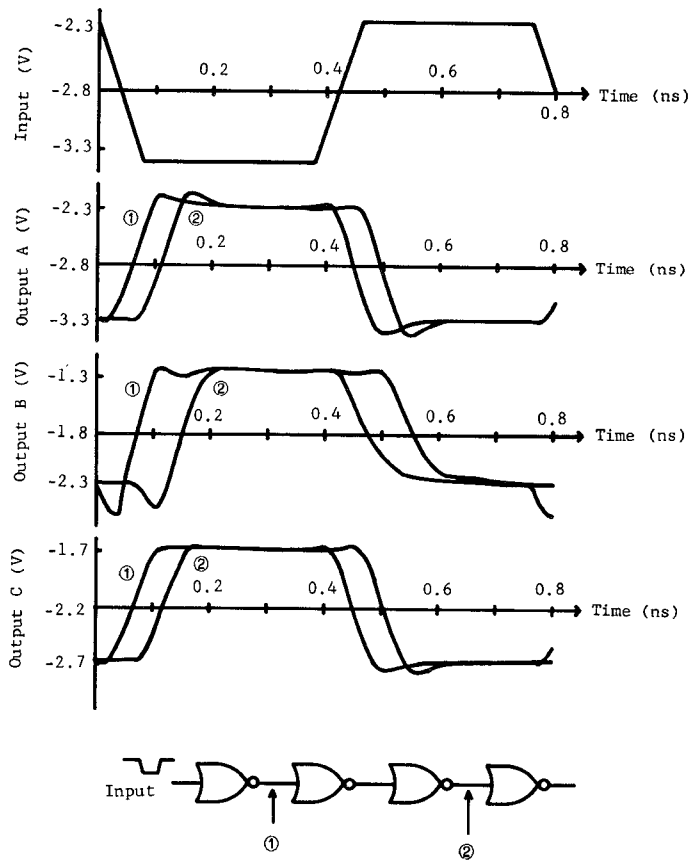


Fig. 10. High-speed pulse response for an SCFL and schematic diagram of the estimation of a chain of two logic gates in four-stage SCFL (calculated).

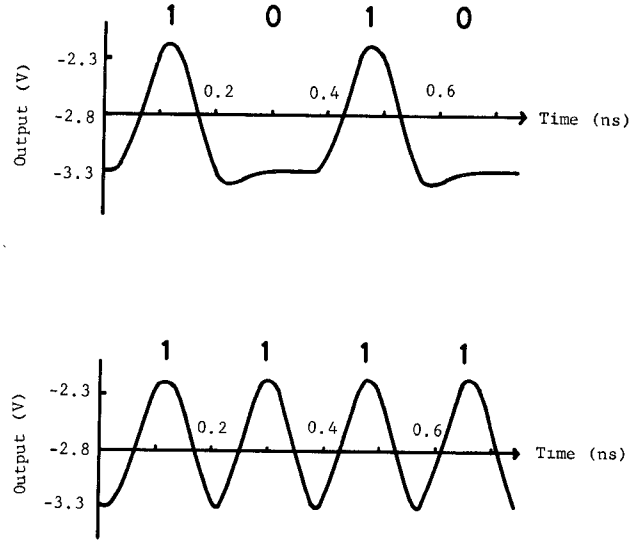


Fig. 11. 5.6 Gb/s RZ data response for SCFL OR gate (calculated).

1010, ···, and 1111, ···, are fed to the same SCFL inverter, under the conditions that waveform A in Fig. 10 is generated, pulse sequence response is shown in Fig. 11. Input pulse conditions, rise time, fall time, and duration are 64 ps, 64 ps, and 180 ps, respectively. Single-current RZ data rate is 5.6 Gb/s. The SCFL circuit is capable of responding to gigabit data.

IV. Conclusion

A source-coupled FET logic (SCFL) circuit is proposed. SCFL circuit performances can be optimized by reference voltage. The speed of an SCFL gate depends on the operating region of the FET. For high-speed operation, the FET's drain-to-source voltage, higher than its pinchoff voltage, has to be supplied. It is hard for a GaAs MESFET, in conventional circuits BFL, SDFL, and DCFL, to operate under this high-speed operating condition. SCFL, which consists of 1.5-μm gate length FET's, shows that minimum propagation time is 25 ps/gate. Minimum rise time and minimum fall time are 54 ps and 51 ps, respectively. Maximum single-current RZ data rate is 5.6 Gb/s. The SCFL circuit is one of the candidates for gigabit logic.

Appendix I
Transition Frequency f_T

A small signal equivalent circuit is shown in Fig. 12. Hybrid parameter h_{21} is given by

$$h_{21} = \frac{g_m j\omega C_{gd}}{\omega^2 C_{gs} R_i + j\omega(C_{gs} + C_{gd})} \tag{A1}$$

where ω is an angular frequency. When $\omega^2 C_{gs}^2 R_i \ll \omega(C_{gs} + C_{gd})$ and $g_m \gg \omega C_{gd}$ at low frequency, $|h_{21}|$ is obtained as follows:

$$|h_{21}| \simeq \frac{g_m}{\omega(C_{gs} + C_{gd})}. \tag{A2}$$

When $|h_{21}| = 1$, f_T is expressed by

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})}. \tag{A3}$$

Appendix II
Details of High-Speed Operation Analysis

Transfer characteristic of the SCFL in Fig. 1 is approximately expressed in Fig. 13. The upper curves are the response of the current switch section only, and the lower curves are the response of the complete SCFL gate. Points P and R are the onset of high-level output. Intersections P' and R' indicate a stable high output level. Points Q and S are the onset of low-level output. Intersections Q' and S' indicate a stable low output level. V_{ref} is the logic threshold voltage. The drain voltage and current which correspond to each operating point in Fig. 13 are shown in Fig. 14. Each load for FET_1 and FET_2 is not equal to R_{L_1} and R_{L_2} because each source potential changes during current switching. Drain-to-source voltage for FET_1 is the smallest when a high voltage level is applied at FET_1 gate. The reason is that FET_2 is switched off and FET_2 source voltage increases. Minimum FET_1 drain-to-source voltage $V_{ds(\min)}$ is represented by the difference between drain voltage and source voltage. FET drain voltage V_{d_1} and source voltage V_{s_1} are given as follows, respectively:

$$V_{d_1} = -V_R - V_{sw} \tag{B1}$$

$$V_{s_1} = V_{\text{ref}} + 0.5V_{sw} - V_{gs_1} \tag{B2}$$

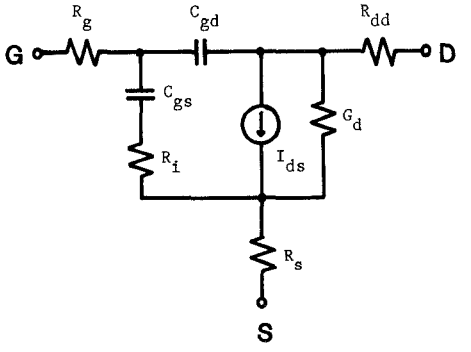


Fig. 12. MESFET model for small-signal analysis.

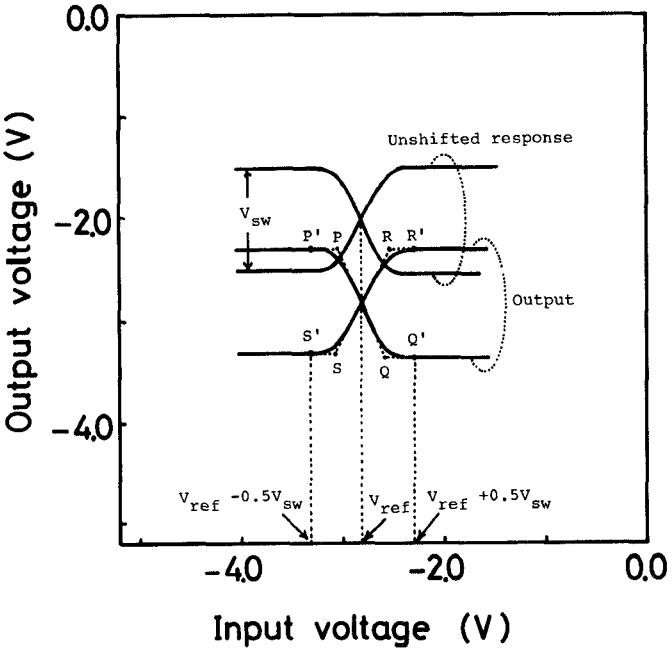


Fig. 13. Approximate dc transfer characteristics for an SCFL OR/NOR gate. Solid lines show unshifted response and the complete response. Broken lines show the output of the following stage.

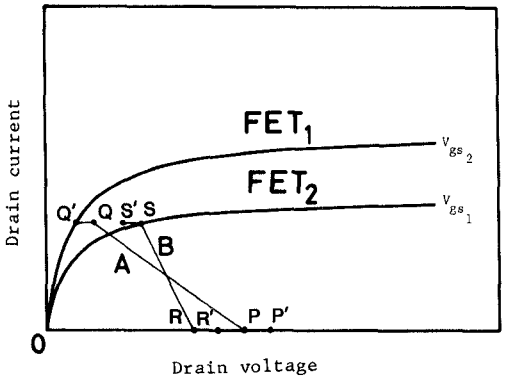


Fig. 14. I–V characteristics for switching FET's, which compose the SCFL gate. Curve A is the load line for FET_1. Curve B is the load line for FET_2.

where V_R is the voltage drop across resistor R. V_{gs_1} is the FET_1 gate-to-source voltage. $V_{ds(\min)}$ is obtained as follows:

$$V_{ds(\min)} = -V_R - 1.5V_{sw} - V_{\text{ref}} + V_{gs_1}. \tag{B3}$$

Drain-to-source voltage within the pinchoff region is

larger than $(V_{gs} - V_{th})$. Consequently, V_{th} is given as follows:

$$V_{th} \geq 1.5V_{sw} + V_R + V_{ref}. \quad \text{(B4)}$$

In the source–follower stage, drain-to-source voltage $V_{ds(sf)}$ for FET_4 and FET_5 is the smallest when the output voltage level is high. For $V_{ds(sf)}$ to become larger than pinchoff voltage, $(V_{gs(sf)} - V_{th(sf)})$

$$V_{ds(sf)} \geq V_{gs(sf)} - V_{th(sf)} \quad \text{(B5)}$$

where $V_{ds(sf)}$ is the sum of V_R and gate-to-source voltage $V_{gs(sf)}$ is this stage, then

$$V_{th(sf)} \geq -V_R. \quad \text{(B6)}$$

Drain-to-source voltage $V_{ds(cs)}$ for FET_3, FET_6, and FET_7, which act as current sources, is the smallest at a low input voltage level and largest at a high input voltage level. When the input voltage level is low and FET_2 gate-to-source voltage is $V_{gs(on)}$, minimum $V_{ds(cs)}$ is given as follows:

$$V_{ds(cs)} = V_{ref} - V_{gs_2(on)} - (-E) \quad \text{(B7)}$$

where E is a supply voltage. Drain-to-source voltage within a pinchoff region is larger than $(V_{cs} + E - V_{th(cs)})$. Consequently,

$$V_{th(cs)} \geq V_{cs} - V_{ref} + V_{gs_2(on)}. \quad \text{(B8)}$$

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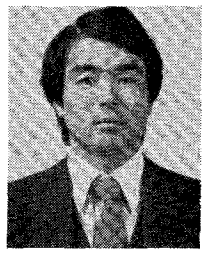

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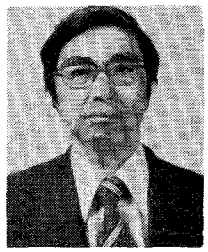

Tsuneta Sudo was born in Tokyo, Japan, on February 3, 1938. He received the B.S. degree and the M.S. degree in electrical engineering from Keio University, Tokyo, Japan, in 1962 and 1964, respectively.

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